REMARKS

Claims 1-14 and 25-31 remain in the application. Claims 15-24 have been canceled. Applicants affirm the election of the species of Group I, i.e., claims 1-14 and 25-31. Reconsideration of the application as amended is requested.

Claims 1, 2 and 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Shino, U.S. Patent No. 5,256,894. Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shino in view of Chou, U.S. Patent 5,272,099. Claims 5, 6 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shino in view of Chou, and further in view of Gardiner, U.S. Patent 4,354,309. Claims 9-14, 25 and 27-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shino in view of Chou and Gardiner, and further in view of Yeh, U.S. Patent 5,840,607. Claim 26 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Shino in view of Chou, Gardiner and Yeh, and further in view of Hong, U.S. Patent 5,352,619. Applicants traverse the rejections because (i) there is no motivation or suggestion contained in the references to combine them, (ii) combining the references does not provide the invention as recited in the claims, (iii) the references teach away from the invention as recited in the claims and (iv) main intents of the references are destroyed in attempting to combine them to provide the claimed invention.

Shino does not teach a floating gate transistor. Shino teaches (col. 1, lines 6-11) a semiconductor device that includes a MOS transistor having a gate electrode formed as a layer of a refractory metal silicide formed over a polysilicon layer. A main intent of Shino is to obviate formation of bird's beaks (see, e.g., 410, Fig. 4C) due to differences in oxidation rate of the silicide and the polysilicon gate layers. This main intent is destroyed when the teachings of Shino are used to try to arrive at the limitations of applicant's base claims 1, 9 and 25. One reason for this is that the metal silicide layers required by Shino are not used in floating gate transistors, obviating the bird's beak formation of Shino. It is improper to employ a reference in a fashion that destroys a main intent of the reference. For at least this reason, the rejection of claims 1-14 and 25-31 is defective and should be withdrawn.

Chou teaches a method for forming a transistor. In this method, the gate polysilicon is formed as two distinct layers 16 and 20 (Figs. 3-5) having different doping characteristics. However, subsequent heat treatment is used "to cause the critical even distribution of dopant in layers 16 and 20" (col. 4, lines 7-16) resulting in a uniformly doped gate electrode 34 (Figs. 6-8; front page illustration). This main intent of Chou is destroyed in attempting to modify the teachings of Chou to arrive at the claimed invention. For at least this reason, the rejection

of claims 3-6, 8-14 and 25-31 is defective and should be withdrawn, and these claims should be allowed.

Gardiner teaches (see Title, Abstract, Description of the Prior Art) that void formation in polysilicon gates is due to presence of dopants in the polysilicon and leads to unacceptably low yields. It is a main intent of Gardiner to improve yields by forming a first, undoped polysilicon layer adjacent the gate oxide and then forming a second, more heavily doped polysilicon layer atop the first layer (see Abstract; col. 1, lines 37-59; col. 2, line 54 through col. 3, line 13). Gardiner also teaches that the process is further improved when the second polysilicon layer has only a relatively moderate impurity concentration and a third layer 12 has a relatively heavy impurity concentration (col. 3, lines 38-43).

Gardiner thus teaches directly away from providing a greater impurity concentration in the first portion and a lesser impurity concentration in the second layer, as recited in all of applicant's claims. For at least this reason, the rejection of claims 5, 6, 8-14 and 25-31 is defective and should be withdrawn, and these claims should be allowed.

Moreover, it is a main intent of Gardiner to provide a sharply reduced impurity concentration in the first layer. Gardiner states (col. 2, lines 59-61) that "The intrinsic nature of the polycrystalline silicon layer 10 is critical to the present invention ...." and that (col. 3, lines 24-26) "The substantially intrinsic nature of the initial polycrystalline

layer 10 provides the important advantages of the present invention." This main intent is destroyed in adapting the teachings of Gardner to arrive at the invention as defined by any of applicant's claims. It is improper to employ a reference in a fashion that destroys a main intent of the reference. For at least this reason, the rejection of claims 5, 6, 8-14 and 25-31 is defective and should be withdrawn, and these claims should be allowed.

Yeh teaches (see Title, Abstract, col. 2, lines 2-7 and 18-20; col. 3, lines 10-14 etc.) a floating gate structure formed from an undoped polycrystalline layer, a doped polycrystalline layer and an undoped polycrystalline layer. It is a main intent of Yeh to provide undoped polycrystalline silicon at both the top and the bottom of the floating gate. Yeh teaches (col. 1, lines 38-51) that doped polycrystalline silicon can degrade tunnel oxide layers and also that doped polycrystalline silicon oxidizes at a rapid rate, making it difficult to control oxide thicknesses grown on the doped polycrystalline silicon. Yeh teaches (col. 3, lines 25-31) that the smaller grain size of the bottom undoped layer reduces impurity diffusion from the middle doped layer and thus prevents degradation of the tunnel oxide layer.

Yeh teaches away from "forming a first layer of conductively doped semiconductive material over a semiconductive substrate; forming a second layer of substantially undoped semiconductive material over the first layer" as recited in claim 9. Yeh also teaches away from "forming a

first layer of polysilicon over a substrate to a first thickness; doping the first layer ..." as recited in claim 25.

Moreover, Yeh's main intent of providing undoped polycrystalline silicon at both the top and the bottom of the floating gate is destroyed in modifying the teachings of Yeh to arrive at applicant's claimed invention. It is improper to use a reference in a way that destroys a main intent of the reference. For at least these reasons, the rejection of claims 9-14 and 25-31 is defective and should be withdrawn, and claims 9-14 and 25-31 should be allowed.

Dependent claims 2-8, 10-14 and 26-31 are allowable as depending from an allowable base claim and for their own recited features which are neither shown nor suggested by any of the references of record, either singly or in combination with one another.

In view of the foregoing, allowance of claims 1-14 and 25-31 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other that a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

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By: _____
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